Sierra Components, Inc.

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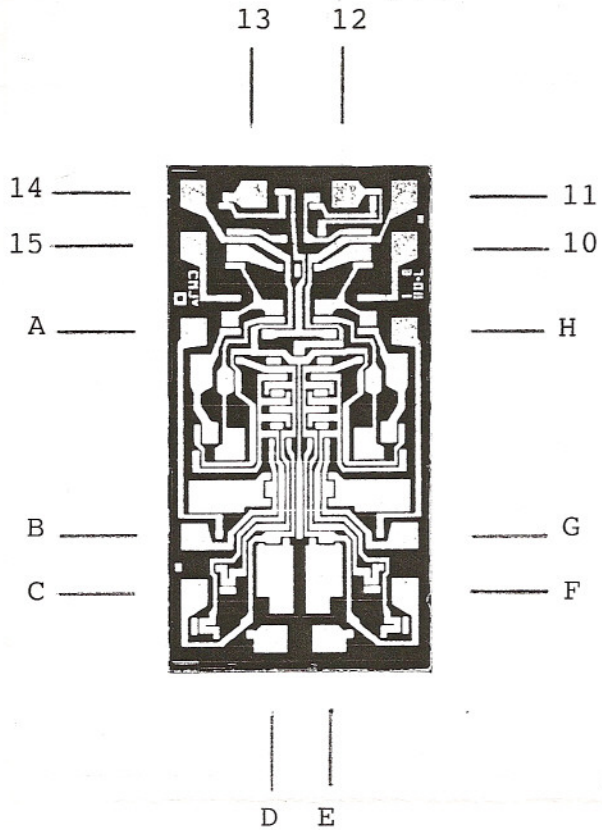
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



INTERCHIP PAD CONNECTIONS	
With 2 JFETs:	
A	No Connection
B	No Connection
C	To JFET 2, Gate
D	From JFET 2, Source
E	From JFET 1, Source
F	To JFET 1, Gate
G	No Connection
H	No Connection
With 4 JFETs:	
A	From JFET 1, Source
B	To JFET 1, Gate
C	To JFET 3, Gate
D	From JFET 3, Source
E	From JFET 4, Source
F	To JFET 4, Gate
G	To JFET 2, Gate
H	From JFET 2, Source

PAD NO.	FUNCTION
10	Input 2
11	V+
12	V_L
13	V_R
14	V- (Substrate)
15	Input 1

CMJB1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG180	NIP1000	2
DG181	NC1000	2
DG182	NC2000	2
DG189	NIP1000	4
DG190	NC1000	4
DG191	NC2000	4

CAUTION
STATIC SENSITIVE
OBSERVE PRECAUTIONS

Topside Metal: Al
Backside: Au
Backside Potential:
Mask Ref:
Bond Pads (Mils):

APPROVED BY:	**DIE SIZE (Mils): 44 x 80**	**DATE: 12/20/99**
MFG: Siliconix	**THICKNESS:**	**P/N: CMJB1000**